

1501

ABSTRACT OF THE DISCLOSURE

The present invention discloses a method and device for ordering memory  
5 operation instructions in an optimizing compiler. The optimizations disclosed  
target processors that can potentially enter a stall state if a memory load operation  
instruction is a cache miss or if a memory queue is full. Disclosed is a new  
optimization method that uses a dependency graph coupled with one or more  
queues. The dependency graph is used to show the dependency relationships  
10 between the instructions in a program being compiled. After creating the  
dependency graph, the ready nodes are identified. At the same time at least one  
queue having a maximum desirable number of elements derived from a target  
processor is made available. Some dependency graph nodes correspond to  
memory operations. Those nodes that do may have the effect of adding an  
15 element to the memory queue or removing one or more elements from the memory  
queue. The ideal situation is keep the memory queue as full as possible without  
exceeding the maximum desirable number of elements, which corresponds to  
scheduling memory operations to prevent maximize the parallelism of memory  
operations while avoiding stalls on the target processor.